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EXAMINER	
ABDULSELAM, ABBAS I	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/829,294	LEE ET AL.	
	Examiner	Art Unit	
	ABBAS I. ABDULSELAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-12,14,16-22 and 24-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-12,14,16-22 and 24-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/13/2008 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-7, 9-12, 14, 16-22 and 24-27 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 20, 24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amundson et al. (USPN 6545291) in view of Ihida et al. (USPN 7075603).

Regarding claims 1 and 24, Amundson et al. (hereinafter = "Amundson") teaches an electrophoretic display (col. 4, lines 54-55), comprising: a first gate line and a second gate line which extend in a first direction (col. 12, line 27, Fig. 5A (310), select line (310), as shown in Fig. 5A, there are two select lines); a first data line and a second data line which extend in a

second direction in a second direction substantially perpendicular to the first direction, (col. 10, line 53, Fig. 5A (330), data line (330) shown in Fig. 5A will be more than one (plural) for more number of pixels as shown in Fig. 5A, the select line (310) is perpendicular to the data line (330)); a first pixel electrode disposed in a first region restricted by the first gate line, second gate line, the first data line, the first data line and the second data line (col. 2, lines 54-58, the pixel electrode and the data line electrode are interdigitated such that the data line electrode comprises a data line of the display, and Fig. 5a (330, 320), Fig. 5A clearly shows that the pixel electrode 320 is between the two select lines 320 and it is quite obvious there has to be another data line parallel to the data line 330 shown in the Fig. as part of a display system),

Amundson does not teach entire lengths of opposing edges defining a first side and a second side of the first pixel electrode along the second direction between the first gate line and the second gate line overlap the first data line and the second data line respectively.

Ihida et al. (USPN 7075603) on the other hand teaches as shown in FIG. 1, that each pixel electrode is divided into a transparent electrode region (10) and a reflection electrode (11) region such that each pixel electrode region is defined by adjacent two scan lines 15 and adjacent two data lines and a reference numeral 14 shows an overlapped portion of a transparent electrode 10 and the reflection electrode 11. Clearly as shown in the figure both edges of the pixel electrode (10, 11) overlaps the two data lines 16.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Amundson's pixel electrode (320) shown in Fig. 5B with Ihida's use pixel electrode (10, 11) as configured in Fig. 1, because the use of such a pixel electrode

helps provide a semi-transmission type liquid crystal display, which is capable of relaxing the positioning preciseness during a fabrication as taught by Ihida.

Regarding claims 20 and 27, Amundson teaches an electrophoretic display (col. 4, lines 54- 55)), comprising; a first gate line and a second gate line which extend in a first direction (col. 12, line 27, Fig, 5A (310), select line (310), as shown in Fig. 5A, there are two select lines); a first data line and a second data line which extend in a second direction in a second direction substantially perpendicular to the first direction, (col. 10, line 53, Fig. 5A (330), data line (330) shown in Fig. 5A will be more than one (plural) for more number of pixels as shown in Fig. 5A, the select line (310) is perpendicular to the data line (330)) a first pixel electrode disposed in a first region restricted by the first gate line, second gate line, the first data line, the first data line and the second data line (col. 2, lines 54-58, the pixel electrode and the data line electrode are interdigitated such that the data line electrode comprises a data line of the display, and Fig. 5a (330, 320), Fig. 5A clearly shows that the pixel electrode 320 is between the two select lines 320 and it is quite obvious there has to be another data line parallel to the data line 330 shown in the Fig. as part of a display system) ; a common electrode (col. 7, lines 43-45, bounding electrodes, col. 8, lines 19-24, multiple pair of electrodes (30, 40) per capsule (20), it is obvious in the electrophoretic display that one of the bounding electrode is a common electrode); and a plurality of micro-capsules (col. 8, lines 39-43, Fig. 1 (20), multiple capsules 20 may be positioned, col. 7, lines 35-38, individual electrophoretic phases may be referred as capsules or microcapsules), wherein each microcapsule of the microcapsules of the plurality of microcapsules comprises electric ink comprising a plurality of color pigment particles, (col. 6, lines 12-19, particles may

be encapsulated in the capsules, and include dyed pigments and are dispersed in a suspending fluid, and col. 7, lines 54-55, Fig. 1A (20, 25, 50), a capsule (20) contains at least one particle (50) dispersed in a suspending fluid (25)), wherein a color of the plurality of color pigment particles is at least one of red, green, blue, cyan, yellow, magenta black and white (col. 8, lines 5-6, particles may be colored any one of a number of colors, and col. 9, lines 31-32, blue particles).

Amundson does not teach entire lengths of opposing edges defining a first side and a second side of the first pixel electrode along the second direction between the first gate line and the second gate line overlap the first data line and the second data line respectively.

Ihida et al. (USPN 7075603) on the other hand teaches as shown in FIG. 1, that each pixel electrode is divided into a transparent electrode region (10) and a reflection electrode (11) region such that each pixel electrode region is defined by adjacent two scan lines 15 and adjacent two data lines and a reference numeral 14 shows an overlapped portion of a transparent electrode 10 and the reflection electrode 11. Clearly as shown in the figure both edges of the pixel electrode (10, 11) overlaps the two data lines 16.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Amundson's pixel electrode (320) shown in Fig. 5B with Ihida's use pixel electrode (10, 11) as configured in Fig. 1, because the use of such a pixel electrode helps provide a semi-transmission type liquid crystal display, which is capable of relaxing the positioning preciseness during a fabrication as taught by Ihida.

Regarding claim 5, Amundson (as modified by Ihida) teaches a thin film transistor comprising a channel (col. 11, lines 36-37, Fig. 4B, a TFT with a channel); a source electrode

(col. 11, lines 6-7, Fig. 5A(120), a source electrode (120)); a drain electrode (col. 11, lines 6-7, Fig. 5A (130), a drain electrode (130)); and wherein the first pixel electrode is made of opaque material and the first pixel electrode overlaps the channel of the thin film transistor (col. 11, lines 45-47, a TFT channel is substantially under the pixel electrode, col. 8, lines 55-56).

5. Claims 14 and 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al.(USPN 7173602) in view of Hanazawa et al. (USPN 5953088) and Ihida et al. (USPN 7075603).

Regarding claims 14 and 26, Hasegawa et al. (hereinafter = "Hasegawa") teaches an electrophoretic display comprising (col. 6, lines 55-56, an electronic ink display,); substrate (col. 9, line 14, Fig. 7 (501) an insulating substrate (501)); and a thin film transistor formed on a surface of the substrate (col. 9, line 9, a TFT) this thin film transistor comprising a source electrode and a drain electrode formed on the substrate (col. 9, lines 11-14, Fig. 7 (403, 501), an electrode layer (403), which is a source- drain electrode formed on an insulating substrate (501)); a semiconductor layer formed on the source and the drain electrode (col. 9, lines 9-14, Fig. 7 (401, 403), the electrode layer (403) and polycrystalline silicon layer (401), col. 9, lines 11- 14, Fig. 7 (403, 501), an electrode layer (403), which is a source-drain electrode formed on an insulating substrate (501)); an insulation layer formed on the semiconductor layer (col. 9, lines 9-10, Fig. 7 (502, 401) a gate insulating film (502) and the polycrystalline silicon layer (401)); and a gate electrode formed on the insulation layer (col. 9, lines 10, Fig. 7 (502, 503), the gate insulating film (502) and gate electrode (503)), a first gate line and a second gate line which

extend in a first direction(col. 10, lines 1-2, Fig. 8 (201) a gate line 201 could be plural); a first data line and a second data line which extend in a second direction substantially perpendicular to the first direction (col. 10, , lines 1-2, Fig. 8 (203), data line (203) could be plural);

Hasegawa does not teach a first pixel electrode disposed in a first region restricted by the first gate line, second gate line, first data line and second data line and a second pixel electrode disposed in a second region adjacent to the first region

Hanazawa on the other hand illustrates as shown in Fig. 3, adjacent two pixel electrodes (51, 54)(PE), a signal line 50a, and a scanning line Y (62') such that parts of the pixel electrodes (51, 54) are inside the signal line (50a) and the scanning line Y (62'). Hence, as can be seen in Fig. 3, portions the pixel electrodes (51, 54) overlap both the signal line (50) and the scanning line Y (62'), and also note that from Fig. 3, pixel electrodes (51, 54) have their respective regions with respect to the signal line 50a and the scanning line Y(62) are (col. 4, lines 11-27).

Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's electrophoretic display shown in Fig. 8 with Hanazawa's pixel electrodes (51, 54) as configured in Fig. 3, because the use of two pixel electrodes helps suppress an increase in the capacitive load of a signal line without impairing an electrostatic shielding property, and obtain a high aperture ratio as taught by Hanazawa (col. 2, lines 19-32).

Hasegawa does not teach entire lengths of opposing edges defining a first side and a second side of the first pixel electrode along the second direction between the first gate line and the second gate line overlap the first data line and the second data line respectively.

Ihida et al. (USPN 7075603) on the other hand teaches as shown in FIG. 1, that each pixel electrode is divided into a transparent electrode region (10) and a reflection electrode (11) region such that each pixel electrode region is defined by adjacent two scan lines 15 and adjacent two data lines and a reference numeral 14 shows an overlapped portion of a transparent electrode 10 and the reflection electrode 11. Clearly as shown in the figure both edges of the pixel electrode (10, 11) overlaps the two data lines 16.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's electrophoretic display shown in Fig. 8 with Ihida's use pixel electrode (10, 11) as configured in Fig. 1, because the use of such a pixel electrode helps provide a semi-transmission type liquid crystal display, which is capable of relaxing the positioning preciseness during a fabrication as taught by Ihida.

6. Claims 7, 11 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drzaic (USPN 6518949) in view of Ihida et al. (USPN 7075603).

Regarding claims 7 and 25, Drzaic (USPN 6518949) teaches an electrophoretic display (col. 1, line 59-61, col. 1, line 67 and col. 2, lines 1-2 and Fig. (8)) comprising; a substrate (Fig. 8(92"), substrate 92'); a first gate line and a second gate line which extend in a first direction (Fig. 7 (106), row electrode 106 could be plural); a first data line and a second data line which extend in a second direction substantially perpendicular to the first direction (Fig. 7 (104), a column electrode 104, as shown in Fig. 7, the column electrode 104 is perpendicular to the row

electrode1 06); a first thin film transistor comprising a first channel (Fig. 8 (90"), transistor (90")); a first gate electrode (col. 10, lines 9, Fig. 8 (96"), gate electrode (96")), a first source electrode (col. 10, lines 7, Fig. 8(98"), source electrode (98")); a first drain electrode and a first semiconductor layer (col. 10, line 8, col. 10, lines 4, Fig. 8(99, 97"), a drain electrode 99"and a semiconductor layer 97"); a first opaque layer (col. 10, line 6, Fig. 8(110) a barrier layer (110), and col. 9, lines 50-51, a barrier layer is opaque) formed on the first semiconductor layer and disposed over the channel of the first thin film transistor (col. 1 O, lines 3-4, the barrier layer (110) is positioned over at least a semiconductor layer (97"), and Fig. 8 (96, 110, 97"), Fig. 8 shows the semiconductor layer 97" is between the gate electrode, 96"and the barrier layer (110)); a second thin film transistor disposed adjacent to the first thin film transistor (Fig. 9 (90"), see Fig. 9 in which the two identical transistor 90' are located adjacent to each other) and comprising a second channel(Fig. 8 (90"), transistor (90")); a second gate electrode (col. 10, lines 9, Fig. 8 (96"), gate electrode (96")); a second source electrode(col. 10, lines 7, Fig. 8(98"), source electrode (98")); and a second drain electrode and a second semiconductor layer (col. 10, line 8, col. 10, lines 4, Fig. 8(99; 97"), a drain electrode 99"and a semiconductor layer 97"); a second opaque layer (col. 10, line 6, Fig. 8(110) a barrier layer (110), and col. 9, lines 50-51, a barrier layer is opaque) formed on the second semiconductor layer and disposed over the channel of the second the film transistor (col. 1 O, lines 3-4, the barrier layer (110) is positioned over at least a semiconductor layer (97"), and Fig. 8 (96; 110, 97"), Fig. 8 shows the semiconductor layer 97" is between the gate electrode, 96"and the barrier layer (11 0)) a first pixel electrode disposed over the first thin film transistor; and a second pixel electrode disposed over the second thin film transistor (col. 2, lines 1 7- 20, use of a plurality of pixel electrodes, col. 9, line 67 and col. 10,

line 1, as shown in Fig. 8 (90, 92, 124), each transistor 90' is positioned adjacent to a pixel electrode 124 on a substrate 92', col. 4, lines 24-25, Fig. 1 (18, 20), it is also known that the transistor (20) are located underneath a pixel electrode 18),

Drzaic (USPN 6518949) does not teach entire lengths of opposing edges defining a first side and a second side of the first pixel electrode along the second direction between the first gate line and the second gate line overlap the first data line and the second data line respectively.

Ihida et al. (USPN 7075603) on the other hand teaches as shown in FIG. 1, that each pixel electrode is divided into a transparent electrode region (10) and a reflection electrode (11) region such that each pixel electrode region is defined by adjacent two scan lines 15 and adjacent two data lines and a reference numeral 14 shows an overlapped portion of a transparent electrode 10 and the reflection electrode 11. Clearly as shown in the figure both edges of the pixel electrode (10, 11) overlaps the two data lines 16.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Drzaic's pixel electrorde 124 shown in Fig. 8 with Ihida's use pixel electrode (10, 11) as configured in Fig. 1, because the use of such a pixel electrode helps provide a semi-transmission type liquid crystal display, which is capable of relaxing the positioning preciseness during a fabrication as taught by Ihida.

Regarding claim 11, Drzaic's (USPN 6518949) teaches wherein the first pixel electrode is made of opaque material (col. 2, lines 38-41, a substrate that can be opaque, and col. 8, lines 15-17, a substrate that can be patterned to serve as the pixel electrode), and wherein the first pixel electrode and the second overlap the channel of the first thin film transistor and the second thin

film transistor respectively (col. 4, lines 23-25, Fig. la (20) the transistors 20 are located underneath the pixel electrodes (18)).

7. Claim 2 and 21 is rejected under 35 U.S.C. 103(a)) as unpatentable over Amundson et al. (USPN 6545291) in view Ihida et al. (USPN 7075603) and further in view of Hanazawa et al. (USPN 5953088).

Regarding claim 2 and 21, Amundson in view of Ihida does not teach a second pixel electrode disposed in a second region adjacent to the first region, wherein the second pixel electrode comprises a first side and a second side opposite the first side, and one of the first data line and second data line overlaps an entire length of an edge of the second pixel electrode defining one of the first side of the second pixel electrode and the second side of the second pixel electrode.

Hanazawa on the other hand illustrates as shown in Fig. 3, adjacent two pixel electrodes (51, 54)(PE), a signal line 50a, and a scanning line Y (62') such that parts of the pixel electrodes (51, 54) are inside the signal line (50a) and the scanning line Y (62'). Hence, as can be seen in Fig. 3, portions the pixel electrodes (51) overlap the signal line (50a).

Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's electrophoretic display (as modified by Ihida) shown in Fig. 8 with Hanazawa's pixel electrodes (51) as configured in Fig. 3, because the use of such a pixel electrode helps suppress an increase in the capacitive load of a signal line without impairing an electrostatic shielding property, and obtain a high aperture ratio as taught by Hanazawa (col. 2, lines 19-32).

8. Claims 3, 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amundson et al. (USPN 6545291) in view Ihida et al. (USPN 7075603) and further in view of Yamamoto et al. (USPN 6563260).

Regarding claims 3, 6 and 22, while Amundson (as modified by Ihida) teaches an insulating layer is/interposed/formed between one of the first data line and second data line and the first pixel electrode(col. 11, lines 17-20, an insulating layer (170) separating a drain electrode (130) from the pixel electrode (320), and col. 10, lines 52-53, Fig. 3 (130, 330), the drain electrode (130) of TFT is connected to a data line 330),

Amundson (as modified by Ihida) does not teach the insulating layer having a dielectric constant lower than approximately 4, with the insulating layer being made of one of a-Si:C:O or a-Si:O:F.

Yamamoto et al. (USPN 6563260) on the other hand teach a dielectric constant of an insulating layer, which could be formed of silicone oxide containing fluorine, being equal or less than 4 as plotted in Fig. 3 (col. 13, lines 59-64 and col. 13, lines 48-50).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Amundson's (as modified by Ihida) insulating layer (170) of an electrophoretic display shown in Fig. 5B with Yamamoto's insulating layer (made of silicone oxide containing fluorine) having less than 4 dielectric constant, because the use of such

insulation layer with a dielectric constant of less than 4 helps manufacture a field emission display whose emitter layer is formed by electrophoresis as taught by Yamamoto (col. 9, lines 9-10, col. 9, lines 16- 18 and col. 13, lines 59-60).

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Amundson et al. (USPN 6545291) in view of Ihida et al. (USPN 7075603) and further view of Izumi et al. (USPN 7148867).

Regarding claim 4, while Amundson (as modified by Ihida) teaches various materials may be used to create electrophoretic displays, and cites as exemplary particles including titania, which may be coated in one or two layers in a metal oxide (col. 6, lines 52-54 and col. 6, lines 61-63),

Amundson (as modified by Ihida) does not teach "one of the first the data line and the second data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti".

Izumi et al. (USPN 7148867) on the other hand teaches source lines (25) may be formed by patterning a metal film of Ta, or Mo as shown in Fig. 1B (col. 8, lines 10-13).

Note that even though Amundson teaches electrophoretic display and Izumi teaches liquid crystal display, the functionality of Amundson's data line (330) and Izmui's source line (25) is the same for both types of displays.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Amundson's data line (330) of an electrophoretic display

shown in Fig. 5A (as modified by Ihida) with Izumi's Tantalum (Ta)-patterned metal film, because the use of Tantalum (Ta)-patterned metal film with respect to source line (25) helps constitute an addressing substrate (IOOB) of display device (100) as taught by Izumi (col. 7, lines 11-13, col. 7, lines 60-61 and col. 8, lines 10- 13).

10. Claims 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable Drzaic (USPN 6518949) in view of Ihida et al. (USPN 7075603) and further in view of Yamamoto et al. (USPN 6563260).

Regarding claims 9 and 12, while Drzaic (as modified by Ihida) teaches an insulating layer formed between one of first the data line and the second data line and one of the first pixel electrode and the second pixel electrode (col. 4, lines 61-65, Fig. 1 C (18; 21, 15"), a pixel electrode (18") and a column electrode 15"and insulator (21) are configured),

Drzaic (as modified by Ihida) does not teach the insulating layer having a dielectric constant smaller than approximately 4 with the insulating layer being made of one of a-Si:C:O or a-Si:O:F.

Yamamoto et al. (USPN 6563260) on the other hand teach a dielectric constant of an insulating layer, which could be formed of silicone oxide containing fluorine, being equal or less than 4 as plotted in Fig. 3 (col. 13, lines 59-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Drzaic's (as modified by Ihida) insulator (21) of an electronic display shown in Fig. lc with Yamamoto's insulating layer (made of silicone oxide containing fluorine) having less than 4 dielectric constant, because the use of such insulation

layer with a dielectric constant of less than 4 helps manufacture a field emission display whose emitter layer is formed by electrophoresis as taught by Yamamoto (col. 9, lines 9-10, col. 9, lines 17-19 and col. 13, lines 59-60).

11. Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Drzaic (USPN 6518949) in view of Ihida et al. (USPN 7075603) and further in view of Izumi et al. (USPN 7148867).

Regarding claim 10, while Drzaic (as modified by Ihida) teaches formation of column electrodes through conductive coatings, which may be Indium, Tin Oxide (IT(?) or some other suitable conductive material (col. 11, lines 10-13, col. 11, lines 19-20),

Drzaic (as modified by Ihida) does not specifically teach "one of the first the data line and the second data line is made of metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti".

Izumi et al. (USPN 7148867) on the other hand teaches source lines (25) that may be formed by patterning a metal film of Ta, or Mo as shown in Fig. 1B (col. 8, lines 10-13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Drzaic" s (as modified by Ihida) column electrode (104) of an electronic display shown in Fig. 7 with Izumi's use of Tantalum -patterned metal film for source lines, because the use of Tantalum (Ta)-patterned metal film with respect to source line (25) helps constitute an addressing substrate (IOOB) of a display device (100) as taught by Izumi.

12. Claim 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Hanazawa et al. (USPN 5953088) and Ihida et al. (USPN 7075603) and further in view of Yamamoto et al. (USPN 6563260).

Regarding claims 16 and 19, While Hasegawa (as modified by Hanazawa and Ihida) teaches an insulating layer is formed between one of the data line and second data line and one of the first pixel electrode and the second pixel electrode, (col. 9, lines 10-11, col. 9, lines 15-16, col. 10, lines 5-6, Fig. 7 (403, 502, 504, 405), an electrode layer (403), interlayer insulating film (504) & gate insulating film (502), and pixel electrode (405)),

Hasegawa (as modified by Hanazawa and Ihida) does not teach the insulating layer has a dielectric constant smaller than approximately 4.

Yamamoto et al. (USPN 6563260) on the other hand teach a dielectric constant of an insulating layer, which could be formed of silicone oxide containing fluorine, being equal or less than 4 as plotted in Fig. 3 (col. 13, lines 59-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's (as modified by Hanazawa and Ihida) insulating films (502, 504) of an electrophoretic display shown in Fig. 7 with Yamamoto's insulating layer (made of silicone oxide containing fluorine) having less than 4 dielectric constant, because the use of such insulation layer with a dielectric constant of less than 4 helps manufacture a field emission display whose emitter layer is formed by electrophoresis as taught by Yamamoto (col. 9, lines 9-10, col. 9, lines 17-19 and col. 13, lines 59-60).

13. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Hanazawa et al. (USPN 5953088) and Ihida et al. (USPN 7075603) and further in view of Izumi et al (USPN 7148867).

Regarding claim 17, while Hasegawa (as modified by Hanazawa and Ihida) teaches electrode layers including a layer of titanium (col. 3, lines 53-55),

Hasegawa (as modified by Hanazawa and Ihida) does not specifically teach "one of the first data line and second data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti".

Izumi et al. (USPN 7148867) on the other hand teaches source lines (25) may be formed by patterning a metal film of Ta, or Mo as shown in Fig. 1B (col. 8, lines 10-13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's (as modified by Hanazawa and Ihida) data line (203) of an electrophoretic display shown in Fig. 8 with Izumi's Tantalum (Ta)-patterned metal film, because the use of Tantalum (Ta)-patterned metal film with respect to source line (25) helps constitute an addressing substrate (IOOB) of display device (100) as taught by Izumi (col. 7, lines 11-13, col. 7, lines 60-61 and col. 8, lines 10-13).

14. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Hanazawa et al. (USPN 5953088) and Ihida et al. (USPN 7075603) and further in view of Hirota (USPN 7098980).

Regarding claim 18, Hasegawa (as modified by Hanazawa and Ihida) does not teach "the inclination angle of the first gate line, the second data line, the first data line and the second data line relative to a surface substrate range s from between approximately 20 degrees to approximately 80 degrees".

Hirota (USPN 7098980) on the other hand teaches as a scanning line (1), pixel electrodes 5 and a common electrode 6 are so configured as to be bent relative to the alignment direction of N-type liquid crystal. Hirota further teaches that the bent angle 10 can be selected to be an angle with the best display performance as long as the angle is within the range from 60 degrees to 120 degrees except 90 degrees (col. 5, lines 28-34, Fig. 5 (1, 5, and 6)).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's (as modified by Hanazawa and Ihida) gate lines (201) of a display shown in Fig. 8 with Hirota's bendable electrode having a range of bending angle (60-120 degrees, (90) excepted), which includes a range of 60-80 degrees, because the use of bendable electrode or line makes it possible to achieve a large screen, wide visual angle display with high yield and low cost as taught by Hirota (col. 5, lines 65-67).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is 571-272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu, can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the

status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Abbas I Abdulselam/

Primary Examiner, Art Unit 2629

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